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Monolithic Uncooled 8 × 8 Bolometer Arrays Based on Poly-SiGe Thermistor

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Abstract This paper presents a monolithic uncooled 8 × 8 bolometer array with polycrystalline silicon-germanium (poly-SiGe) thermistors as active elements. The poly-SiGe films are deposited by ultrahigh vacuum vapor deposition (UHV/CVD) system and the dependence of the temperature coefficient of resistance (TCR) on annealing temperature has been investigated. To decrease the thermal conductance of the bolometer, the poly-SiGe thermistor was formed on a four leg suspended microbridge. The improved porous silicon micromachining techniques described here enable the integration of the bolometer array with the MOS readout circuitry. The measurements and calculations show that the mean responsivity is 1.07×10^4 V/W with an uncorrected uniformity of 10.5% and a thermal response time of 10.5 ms, and the detectivity of 3.75×10^8 cm $Hz^{1/2}$/W is achieved at a chopping frequency of 30 Hz and a bias voltage of 5 V.

Keywords Bolometer · Poly-SiGe · Porous silicon micromachining · Integration approach

Introduction

Uncooled Infrared (IR) detectors have potential for use in a variety of military and commercial applications and have developed rapidly in recent years [1–8]. They were usually fabricated by combining silicon IC processes and micromachining techniques. There are primarily three types of infrared detectors: bolometer, pyroelectric and thermopile-based. Regardless of the detection mechanism, the temperature sensitivity of the active element and the thermal isolation of the device are among the important factors of achieving high responsivity. Monolithic uncooled IR detector arrays offer the possibility of a significant reduction in the cost and complexity of IR imaging systems, opening the way for large-scale utilization of infrared sensor technology.

Up to now, a wide variety of materials have been used as active elements for bolometers. Vanadium oxide (VO_x) is the most widely used due to its high temperature coefficient of resistance (TCR) of −2 to −3% $°C^{-1}$ and its low temperature process [8]. The main drawback of VO_x is that it is not a standard material in IC fabrication processes. Boron-

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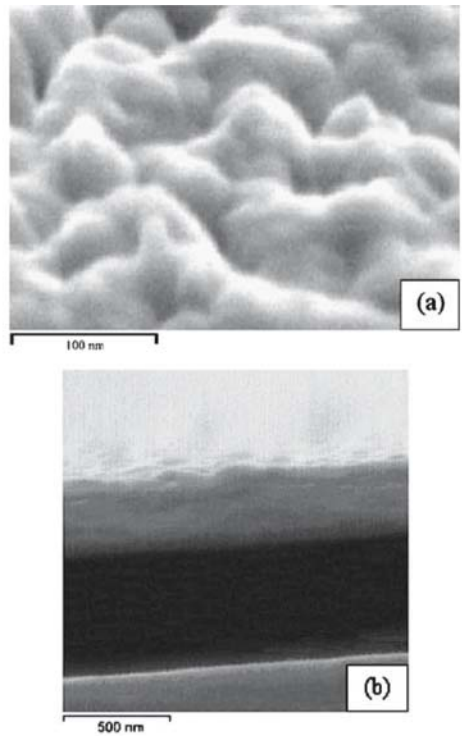

Fig. 1 SEM surface morphology of the poly-SiGe film, (a) *top view*. (b) *cross-sectional view*

doped amorphous silicon (a-Si:B) is a commonly used IC compatible material which has an attractive TCR of −2 to −8% $°C^{-1}$, though its excess low frequency noise compromises the TCR [9]. To achieve good thermal isolation of the device, the use of micromachining techniques makes it possible to place an active element on top of a suspended air bridge that is thermally isolated from the bulk substrate. At present, a number of bulk and surface micromachining techniques have been utilized to realize micromachined bridge structures, and some of them can integrate with readout circuitries. Although many groups have reported on micromachining applications of porous silicon, they are generally concerned about either formation and etching of porous silicon or overcoming geometrical limitations of the

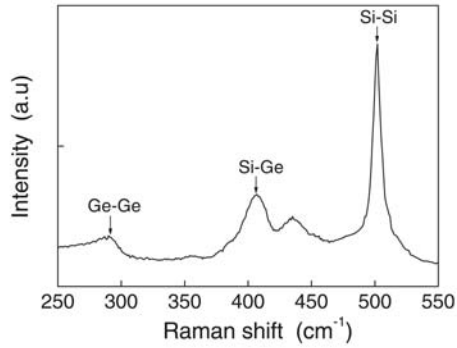

Fig. 2 Raman spectra of the poly-SiGe film

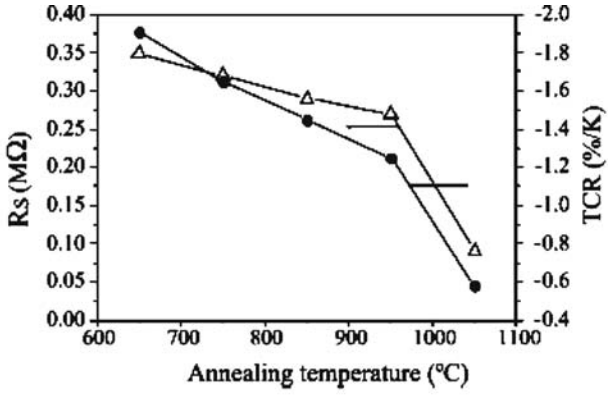

Fig. 3 Dependence of the resistance and TCR on the annealing temperature

freestanding membranes. To our knowledge, there are few reports on integration schemes of combining porous silicon micromachining process for MEMS-structures with the standard IC process for smart electronics.

Recently, polycrystalline silicon-germanium (poly-SiGe) films have attracted great interests in a variety of applications. Since the melting point of SiGe alloy is lower than that of Si, one advantage of poly-SiGe film is that it requires lower thermal budget for

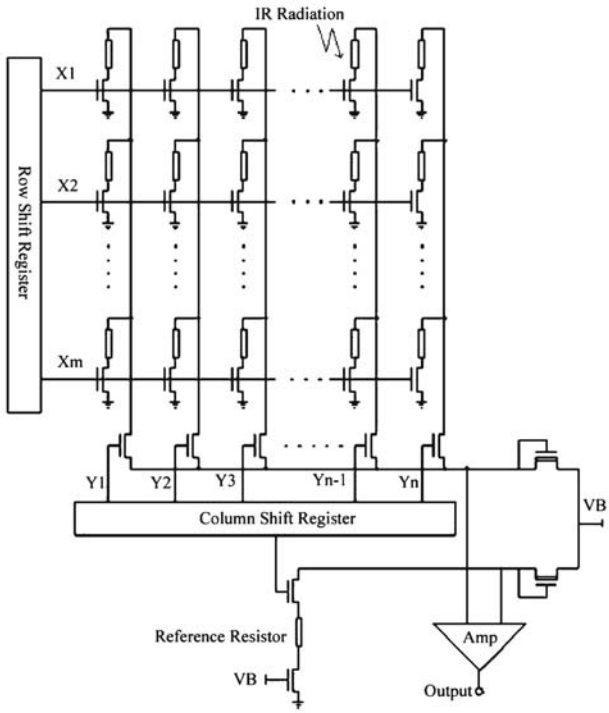

Fig. 4 Circuit configuration of 8 × 8 bolometer array

crystallization, grain growth and dopant activation, thus occurring at lower temperature, than poly-Si film [10]. Additionally, the thermal conductivity of the poly-SiGe alloy is lower than that of poly-Si. For a germanium mole fraction of 30%, it is at least a factor of four lower than that of poly-Si [11]. In this paper, we chose poly-SiGe as the thermosensitive material and an integrated 8 × 8 bolometer arrays were fabricated using a novel integration approach as follows: a sacrificial material of porous silicon is prepared in the first step, then it is well protected all the time during the fabrication of MOSFETs and bolometers before being released. This method is different from the commonly front-end CMOS process and back-end micromaching process, enabling ease of preparing and releasing porous silicon sacrificial layer and fabricating monolithic bolometer arrays with a readout circuitry.

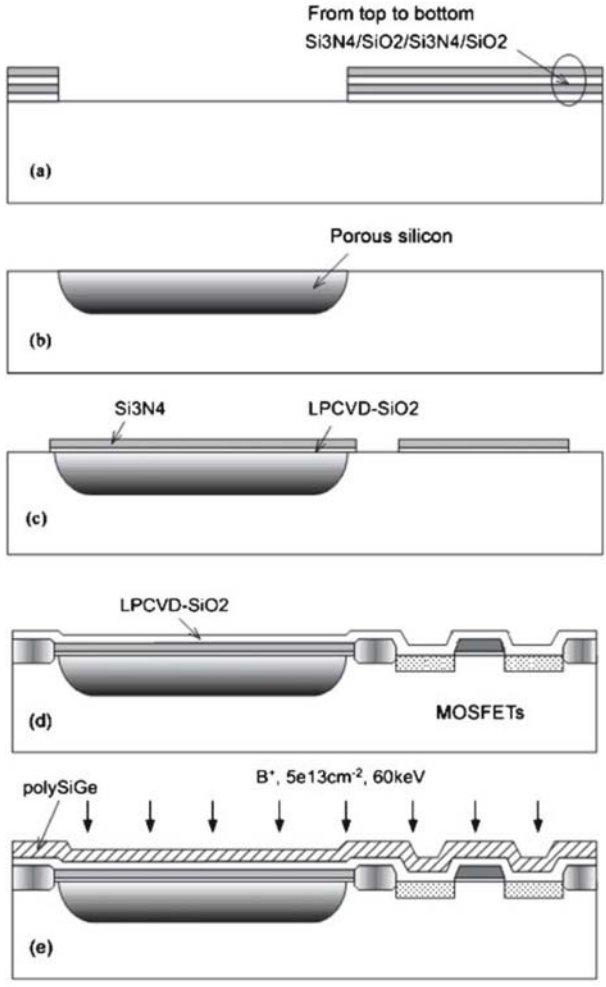

Fig. 5 Process flow of an bolometer array

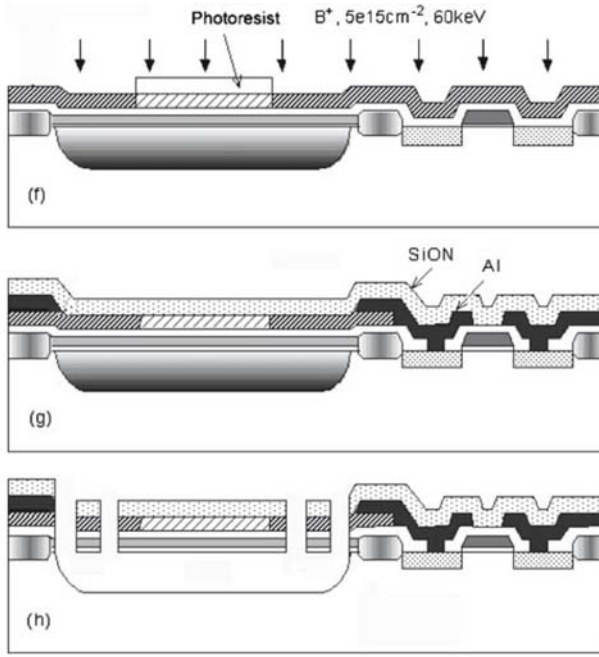

Fig. 5 Continued

Properties of the Poly-SiGe Film

The poly-SiGe film was deposited on a three-inch silicon wafer by an ultrahigh vacuum vapor deposition (UHV/CVD) system described in somewhere else [12]. Prior to deposition, the growth chamber was evacuated to a base pressure of below 1.0×10^{-7} Pa. The deposition was carried out at a temperature of 550°C and a chamber pressure of 2.5×10^{-2} Pa, with flow of 15 sccm for SiH_4 and 4.4 sccm for GeH_4. After deposition, poly-SiGe films were doped through ion implantation with two different boron doses: 5×10^{13} and 5×10^{15} cm^{-2}

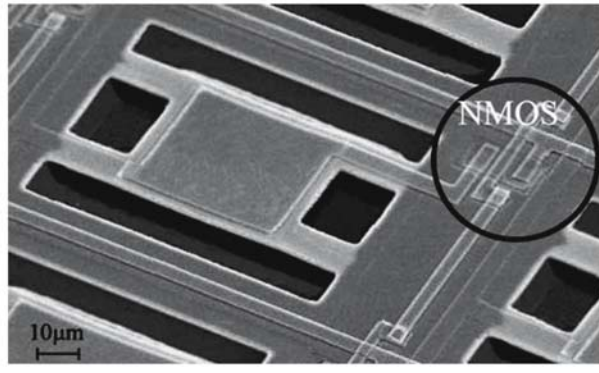

Fig. 6 *Top view* photo of a fabricated bolometer pixel

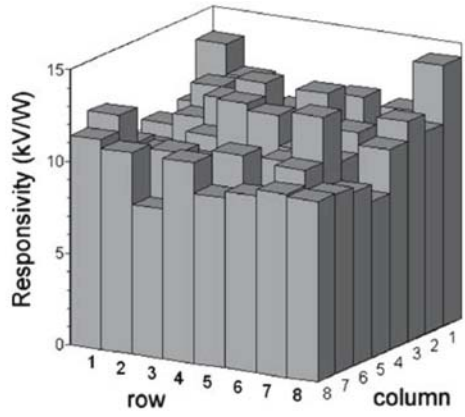

Fig. 7 Distributions of voltage responsivity of a 8 × 8 bolometer array

with the same implant energy of 60 keV, and subsequently annealed at different temperatures ranging from 650 to 1,050°C for 1 min in N_2 ambient within a rapid thermal annealing (RTA) reactor.

Figure 1 is the SEM surface morphology of the deposited poly-SiGe thin film, indicating the formation of a polycrystalline film with the film thickness of 0.3 μm. The poly-SiGe grains nestle together with the approximate grain size of several dozens of nanometers. Rutherford backscattering spectrometry (RBS) measurement shows that the prepared poly-SiGe film has a Ge mole fraction of 0.29. Figure 2 displays the typical Raman spectra of as-deposited poly-$Si_{0.71}Ge_{0.29}$. The three Raman peaks representing the Si–Si, Si–Ge and Ge–Ge phonon modes located at 288, 405 and 501 cm^{-1}, respectively, are clearly visible.

Figure 3 shows the dependence of the sheet resistance *R*s and TCR on the annealing temperature for film with lightly doping dose of 5×10^{13} cm^{-2}. It is indicated that, both resistance and TCR decrease approximately linearly and not sharply until the annealing temperature reaches 950°C, then both two drop distinctly. This may be due to the recrystallization at higher annealing temperature, forming a large crystal and reducing the total grain boundary area available to trap carriers in poly-SiGe. Thus, the activation energy must be reduced strongly, which results in a distinct drop of the resistance and TCR at 1,050°C. Figure 3 also presents that 650°C is enough to activate the boron dopant in poly-SiGe, which is helpful to reduce the highest temperature of bolometer process. For

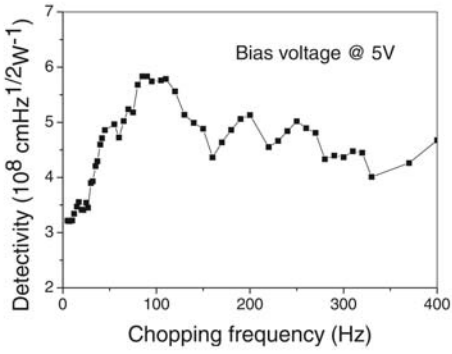

Fig. 8 Dependence of the detectivity on the chopping frequency

poly-SiGe with annealing at 650°C, *R*s is 0.35 MΩ and TCR is $-1.91\%K^{-1}$ at 296 K. While for film with a heavily doping dose of 5×10^{15} cm^{-2} and annealing at 650°C, *R*s and TCR are 0.92 kΩ and a positive value of $0.09\%K^{-1}$, respectively, indicating that such a heavy dose gives a low resistance and a negligible TCR and is suitable for electrical contacts of resistor.

Array Circuitry Design

The circuit configuration of the 8 × 8 bolometer array is shown in Fig. 4, which is composed of vertical and horizontal shift registers, and a preamplifier. The whole chip has an area of 2.7 × 2.6 mm in a 1 μm NMOS process. The multiplexing operations are used to allow individual addressing of the pixels. Since the currently fabricated array is a small-scale demonstrator prototype, serial readout approach is selected for simple implementation. A sensing pixel and a reference resistor are selected by incorporating the vertical and horizontal shift registers, and then connected with two MOSFET load elements to form a Wheatstone bridge. The reference resistor identical to the sensing thermistor is placed within the silicon substrate. During several microseconds readout time, thermistor change of the sensing pixel due to self-heating and ambient temperature variations is compensated by that of the reference resistor.

Fabrication

The main fabrication procedures are shown in Fig. 5. (100)-oriented p-type silicon wafers (3 inch, 1–10 Ω cm resistivity) were used as the starting substrates. First, a composite membrane consisting of 50 nm thermal grown SiO_2 layer and 300 nm Si_3N_4/50 nm SiO_2/250 nm Si_3N_4 layers deposited by low-pressure chemical vapor deposition (LPCVD) was used as the masking layer against hydrofluoric acid (HF) during porous silicon formation. Then, windows were opened on the masking layer [Fig. 5(a)] and the porous silicon was prepared using conventional anodization methods. It was carried out in a solution of 20% wt. HF, 30% water and 50% alcohol with a constant current of 30 mA/cm^2 for 55 min, and the thickness of the prepared porous silicon layer was about 16.5 μm. Later on, the wafer was immersed into a 40% wt. HF solution to remove the masking layer [Fig. 5(b)], and a protective membrane consisting of 50 nm SiO_2 and 150 nm Si_3N_4 was deposited by LPCVD and patterned to seal the porous silicon surface [Fig. 5(c)]. After n-MOSFETs were

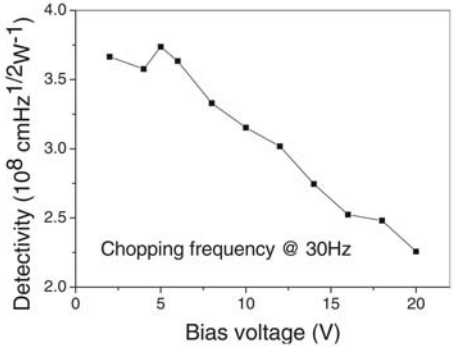

Fig. 9 Dependence of the detectivity on the bias voltage

fabricated, a 500 nm LPCVD SiO_2 was then deposited over the circuit to form a flat surface [Fig. 5(d)]. This film was combined with the Si_3N_4 (150 nm)/SiO_2 (50 nm) protective membrane to form a low-stress sandwich structure to support the postfabricated air bridge. Next, an active layer of 120 nm thick Poly-SiGe film was deposited by UHV/CVD and lightly doped with boron [Fig. 5(e)], and then heavily boron doped using photoresist film as masking layer to cover those areas for thermistors [Fig. 5(f)]. After annealed at 650°C and patterened, a 1.0 μm thick Al film was sputtered and patterned to form the electrical connections of the circuitry. Since the SiON layer has good IR absorptions due to Si–O bonds (8–10 μm) and Si–N bonds (11–13 μm) [13], a 800 nm SiON layer was deposited by PECVD as passivation layer [Fig. 5(g)], and anneal was performed at 350°C for 40 min in a hydrogen ambient. Finally, etching holes were patterned and opened by removal of a stack of films until the top surface of the porous silicon appeared, and the device was completed by releasing the porous silicon sacrificial layer with TMAH solution [Fig. 5(h)]. A fabricated bolometer pixel is shown in Fig. 6.

Performance

The voltage responsivity and noise voltage of the bolometer pixels were measured at atmospheric pressure and an operating temperature of 296 K. The bolometer pixels were connected in series to a dc voltage source and to a load resistance equal to the bolometer resistance. The IR radiation emitted from a blackbody of 700°C was modulated by a mechanical chopper. An optical filter was used to reduce the spectral region of 8–14 μm. The voltage signal was measured using an SR510 lock-in amplifier while the noise voltage was measured using the same system without radiation illumination. The responsivity expression R_V is given by

$$R_V = \eta\beta V \Big/ \left(4G_{\text{th}}\sqrt{1+4\pi^2 f^2\tau^2}\right) \tag{1}$$

where η is the IR absorptance, β is the TCR value, V is the bias voltage, f is the chopping frequency, τ is the thermal time constant, and G_{th} is the thermal conductance. Figure 7 displays the distributions of voltage responsivity of a 8 × 8 bolometer array at 30 Hz. The mean responsivity is 1.07×10^4 V/W with the uncorrected uniformity of 10.5%. Because the thickness nonuniformity of the poly-SiGe films deposited in our UHV/CVD system is usually more than 7% for 3 inch wafers, it must be improved considerably to fabricate a large scale bolometer array. By fitting the measured responsivity using Eq. 1, a thermal time constant of 10.5 ms is attained.

The detectivity D^* is an important figure of merit which takes into account the noise voltage as well as its responsivity, and is given by

$$D^* = R_V\sqrt{A\Delta f}/V_{\text{n}} \tag{2}$$

where A is the area of the pixel, Δf is the measurement bandwidth, V_{n} is the noise voltage. Figure 8 reveals the dependence of calculated detectivity of the bolometer pixel with maximum responsivity on the chopping frequency at a bias voltage of 5 V. It shows that the maximum detectivity of 5.8×10^8 cm $Hz^{1/2}$/W is achieved at a chopping frequency of 90 Hz. Figure 9 gives the dependence of the calculated detectivity on the bias voltage. It shows that the detectivity of 3.75×10^8 cm $Hz^{1/2}$/W is achieved at a chopping frequency of 30 Hz and a bias voltage of 5 V.

Conclusion

We present a novel integration approach based on improved porous silicon micromachining techniques enabling the integration of the bolometer array with the MOS readout circuitry. As one of its applications, a monolithic uncooled 8 × 8 bolometer array with poly-SiGe thermistors as active elements was successfully developed. The detectivity of 3.75×10^8 cm $Hz^{1/2}/W$ is achieved at a chopper frequency of 30 Hz and a bias voltage of 5 V with a thermal response time of 10.5 ms, which is suitable for the frequency response required for 30 Hz imaging applications. To improve the performance of the bolometer arrays, more work must be done about the quality of the poly-SiGe films.

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