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Integrated a-Si:B Microbolometer Arrays Based on Improved Porous Silicon Micromachining Techniques *

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A monolithic uncooled 8×8 microbolometer array with boron-doped a-Si (a-Si:B) thermistors as active elements is presented. The a-Si:B film was deposited by plasma enhanced chemical vapour deposition. To decrease the thermal conductance of the microbolometer, a-Si:B thermistor was formed on a four-leg suspended microbridge. The improved porous silicon micromachining techniques described here enable the integration of the sensor array with the metal–oxide–semiconductor readout circuitry. The sacrificial material of porous silicon is prepared in the first step. It is then well protected all the time during the fabrication of metal–oxide–semiconductor field effect transistors and microbolometers before being released. Measurements and calculations show that the uncorrected uniformity of the 8×8 microbolometer array is about 4.5%, and the detectivity of 2.17×10^8 cm $Hz^{1/2}W^{-1}$ is achieved at a chopping frequency of 30 Hz and a bias voltage of 5 V with a thermal response time of 12.4 ms.

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Infrared detectors and focal plane arrays (IRFPA) play a fundamental role in both civilian and military applications. In recent years, uncooled infrared detectors based on silicon integrated-circuit (IC) processes and micromachining techniques have been developed rapidly.[1−5] They primarily include three types: microbolometer, pyroelectric and thermopile-based. We have chosen the microbolometer type array for our present research not only because its responsivity is higher than that of thermopile detectors, but also it is generally easier to fabricate than pyroelectric detectors, and IR chopping is not necessary. In addition, regardless of the detection mechanism, the temperature sensitivity of the active element and the thermal isolation of the device are among the important factors of achieving high responsivity, and it is preferred to integrate with readout circuitry to improve reliability and reduce cost, weight and size.

When choosing the thermosensitive material for the microbolometer, important considerations include a high temperature coefficient of resistance (TCR), low noise and compatibility with the IC fabrication. A wide variety of materials have been used as the active elements for microbolometers. Vanadium oxide (VO_x) is the most widely used due to its high TCR from −2 to $-3\%^\circ C^{-1}$ and its low temperature process.[6] The main drawback of VO_x is that it is not a standard material in IC fabrication processes. It is known that a-Si:B is a commonly used IC compatible material which has an attractive TCR from −2 to $-8\%^\circ C^{-1}$, though its excess low frequency noise compromises the TCR.[7] To achieve good thermal isolation of the device, the use of micromachining techniques makes it possible to place the active element on top of a suspended air bridge that is thermally isolated from the bulk substrate. Up to date, a number of bulk and surface micromachining techniques have been utilized to realize a micromachined bridge structure, and a few of them can integrate with readout circuitries. Although many groups have reported on micromachining applications of porous silicon, they are generally concerned about either formation and etching of porous silicon or overcoming geometrical limitations of the freestanding membrane. To our knowledge, there are few reports on integration schemes of combining porous silicon micromachining process for MEMS-structures with the standard IC process for smart electronics. In this Letter, we chose a-Si:B as the thermosensitive material and the integrated 8×8 microbolometer arrays were fabricated using a novel integration approach as follows: (i) fabrication and protection of porous silicon sacrificial layer (SL); (ii) fabrication of readout circuitry using the standard IC process; and (iii) deposition and patterning of the films for the microbolometers, followed by releasing the SL. This method is different from the commonly front-end CMOS process and back-end micromachining process, enabling ease of preparing and releasing porous silicon SL and fabricating monolithic microbolometer arrays with readout circuitry.

In order to obtain higher TCR and lower excess of low frequency noise, the a-Si:B film was obtained by plasma enhanced chemical vapour deposition (PECVD) with various SiH_4/B_2H_6 gas ratio at substrate temperature of 200–380° and rf power of 10–500 W. Although the TCR increases with the decrease of doping concentration, the thermal noise voltage of the film is proportioned to the square root of the resis-

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tivity ρ and the film with high ρ is difficult to make the contacts between the electrode and it ohmic. Therefore, we define the figure of merit Q for the a-Si:B film as $\mathrm{TCR}/\rho^{1/2}$. From Table 1, we can see that the Q value is the highest when the resistivity and TCR of the film at 23°C are 39.68 Ωcm and $-2.38\%{}^\circ\mathrm{C}^{-1}$ respectively, which is the case of the 180-nm-thick a-Si:B film used in the microbolometer when SiH_4 (concentration is 10% diluted with Argon) flow is 40 sccm, B_2H_6 (concentration is 1% diluted with Hydrogen) flow 9 sccm and rf power 300 W at substrate temperature of 300°C. To decrease the thermal conductance of the microbolometer, a-Si:B thermistor is formed on a four-leg suspended microbridge with a cavity height of 16.5 μm.

Table 1. TCR and Q value of a-Si:B films with various resistivity at 23°C.

Resistivity (Ωcm)	4×10^5	1.2×10^5	1124	400	175.4	64.52	39.68	37.74
$\mathrm{TCR}\%{}^\circ\mathrm{C}^{-1}$	−6.58	−5.71	−3.88	−3.31	−3.19	−2.64	−2.38	−2.31
Q value	0.01	0.017	0.116	0.166	0.24	0.329	0.378	0.376

The circuit configuration of the 8 × 8 microbolometer array is shown in Fig. 1, which is composed of vertical and horizontal shift registers, and a preamplifier. The whole chip has an area of 2.7 mm × 2.6 mm in a 1-μm NMOS process. The multiplexing operations are used to allow individual addressing of the pixels. Since the currently fabricated array is a small-scale demonstrator prototype, serial readout approach is selected for simple implementation. A sensing pixel and a reference resistor are selected by incorporating the vertical and horizontal shift registers, and then connected with two metal-oxide-semiconductor field effect transistor (MOSFET) load elements to form a wheatstone bridge. The reference resistor identical to the sensing thermistor is placed within the silicon substrate. During several microseconds readout time, thermistor change of the sensing pixel due to self-heating and ambient temperature variations is compensated for by that of the reference resistor.

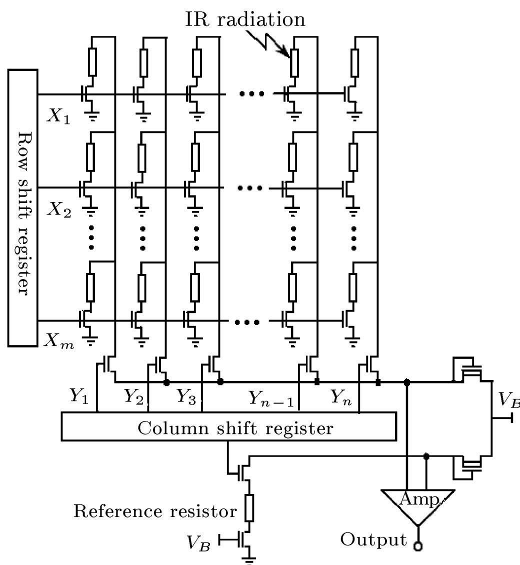

Fig. 1. Circuit configuration of 8 × 8 microbolometer array.

The main fabrication procedures are shown in Fig. 2. Here (100)-oriented p-type silicon wafers (3 inch, 1–10 Ωcm resistivity) were used as the starting substrates. First, a composite membrane consisting of 50 nm thermal grown SiO_2 layer and (300 nm)Si_3N_4/(50 nm)SiO_2/(250 nm)Si_3N_4 layers deposited by low-pressure chemical vapour deposition (LPCVD) was used as the masking layer against hydrofluoric acid (HF) during porous silicon formation. Then, windows were opened on the masking layer and the porous silicon was prepared using conventional anodization methods. It was carried out in a solution of 20 wt.% HF, 30% water and 50% alcohol with a constant current of 30 mA/cm^2 for 55 min, and the thickness of the prepared porous silicon layer was about 16.5 μm. Later on, the wafer was immersed into a 40 wt.% HF solution to remove the masking layer, and a protective membrane consisting of 50 nm SiO_2 and 150 nm Si_3N_4 was deposited by LPCVD and patterned to seal the porous silicon surface [Fig. 2(b)]. Next, n-MOSFETs were fabricated. A 500 nm LPCVD SiO_2 layer was then deposited over the circuit to form a flat surface. This film was combined with the Si_3N_4 (150 nm)/SiO_2 (50 nm) protective membrane to form a low-stress sandwich structure to support the post-fabricated air bridge. After an active layer of 180-nm-thick a-Si:B film for thermistors was deposited by PECVD and patterned [Fig. 2(c)], a 1.0-μm-thick Al film was sputtered and patterned to form the electrical connections of the circuitry. Since the SiON layer has good IR absorptions due to Si-O bonds (8–10 μm) and Si-N bonds (11–13 μm),[8] an 800-nm SiON layer was deposited by PECVD as the passivation layer, the annealing was performed at 350°C for 40 min in a hydrogen ambient [Fig. 2(d)]. Finally, etching holes were patterned and opened by removal of a stack of films until the top surface of the porous silicon appeared, and the device was completed by releasing the porous silicon sacrificial layer with TMAH solution [Fig. 2(e)]. A fabricated 8 × 8 microbolometer array is shown in Fig. 3.

Figure 4 reveals the dependence of detectivity of a microbolometer on the chopping frequency at a bias voltage of 5 V. It shows that the maximum detectivity

of 3.3×10^8 cm $\text{Hz}^{1/2}\text{W}^{-1}$ is achieved at a chopping frequency of 180 Hz. Figure 5 gives the dependence of the detectivity on the bias voltage. It shows that the detectivity of 2.17×10^8 cm $\text{Hz}^{1/2}\text{W}^{-1}$ is achieved at a chopper frequency of 30 Hz and a bias voltage of 5 V with a thermal response time of 12.4 ms. Figure 6 displays the distributions of voltage responsivity of a 8×8 sensor array at 30 Hz. The mean responsivity is 1.64×10^4 V/W with the uncorrected uniformity of 4.5%.

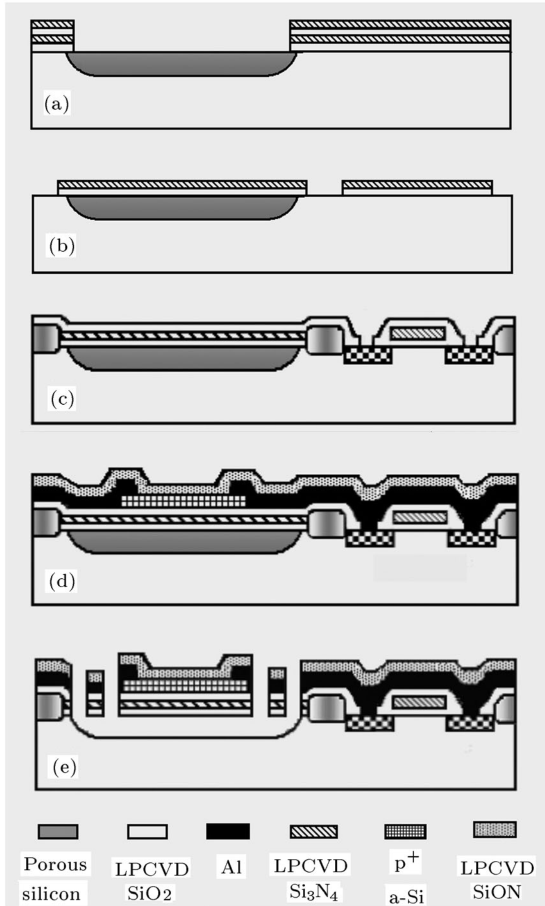

Fig. 2. Process flow.

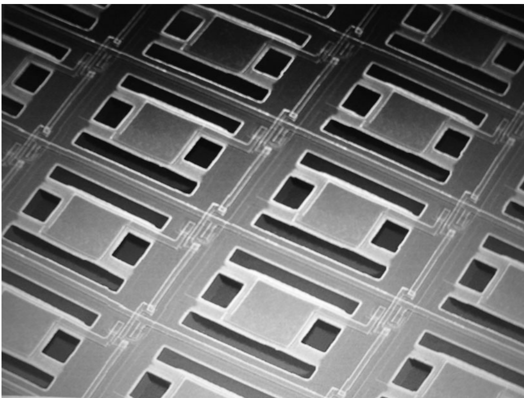

Fig. 3. Micrograph of a 8×8 microbolometer array.

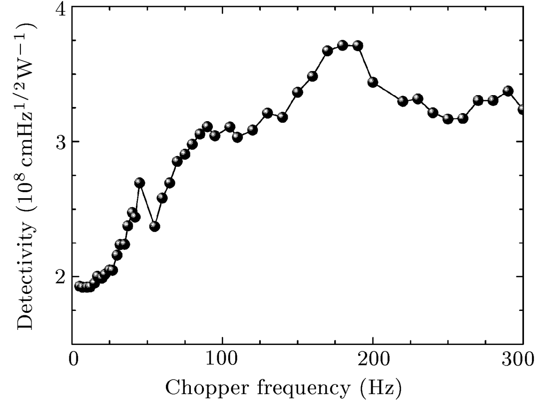

Fig. 4. Dependence of the detectivity on the chopper frequency at dc voltage 5 V.

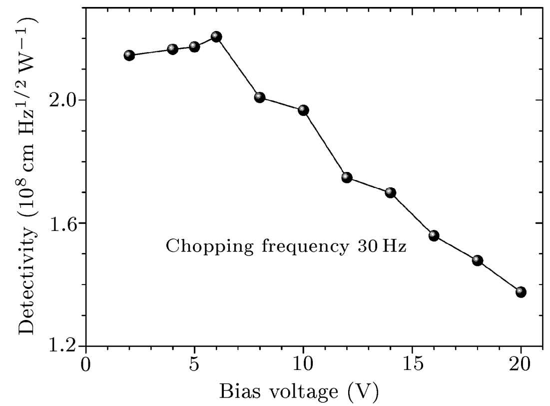

Fig. 5. Dependence of the detectivity on the bias voltage.

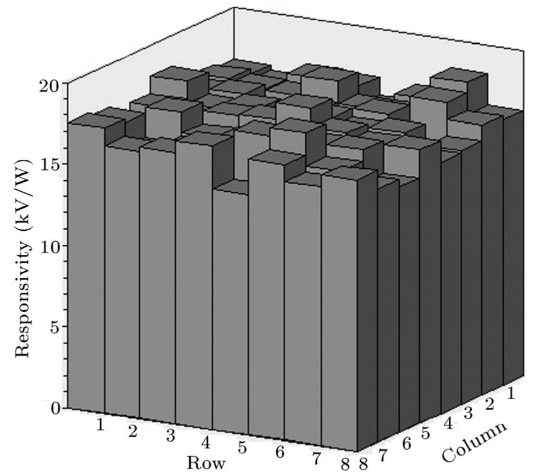

Fig. 6. Distributions of voltage responsivity of an 8×8 sensor array.

In summary, we have presented a novel integration approach based on improved porous silicon micromachining techniques enabling the integration of the sensor array with the MOS readout circuitry. As one of its applications, a monolithic uncooled 8×8 mi-

crobolometer array with a-Si:B thermistors as active elements was successfully developed. Its detectivity of 2.17×10^8 cm $Hz^{1/2}W^{-1}$ is achieved at a chopper frequency of 30 Hz and a bias voltage of 5 V with a thermal response time of 12.4 ms, which is suitable for the frequency response required for 30 Hz imaging applications.

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