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Design and fabrication of single-chip a-Si TFT-based uncooled infrared sensors

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Abstract

This paper reports the theory, fabrication and testing of a novel single-chip uncooled infrared (IR) sensor using amorphous silicon thin film transistors (a-Si TFTs) as the sensing elements. The measured temperature coefficient of drain current of the fabricated a-Si TFT is about 4.8%/K at 23 °C. An integration scheme of combining a standard IC process sequence for forming n-MOSFETs with porous silicon micromachining process is described. Experimental results show that the a-Si TFT-based uncooled IR sensor has a responsivity of over 40 kV/W, a detectivity of over 10^8 cm $Hz^{1/2}$ W^{-1}, a thermal response time of 9.1 ms and a noise equivalent temperature difference of below 0.1 °C at a chopping frequency of 30 Hz.
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Keywords: Uncooled; a-Si TFT; Infrared sensor; Integration; Porous silicon

1. Introduction

Recently, uncooled infrared (IR) sensors have attracted considerable interest due to the wide range of applications at low cost, such as security survey, biomedical thermograph, and fire detection. There are several families of available uncooled IR sensors, such as resistive [1] or dielectric bolometers [2], pyroelectrics [3], thermopiles [4], and other solid-state sensors [5,6]. Each of these uncooled IR sensors can be modeled as a temperature-sensitive element of thermal mass C_{th}, connected to a bulk substrate through a thermal conductance G_{th}. Current efforts focus on enhancing the temperature sensitivity of the sensing element, reducing the thermal conductance of the sensor, and integrating micromachined components with silicon MOS electronics.

In this paper, we present a novel mieromachined uncooled IR sensor based on amorphous silicon thin film transistors (a-Si TFTs). An important reason that the a-Si TFT is useful for IR detections is that it possesses a sensitive temperature dependence of drain current. The measured temperature coefficient of drain current of the fabricated a-Si TFT, i.e. the most significant figure-of-merit of the sensing element, is about 4.8%/K at room temperature. Compared with the temperature coefficient of resistance (TCR) values of some typical materials such as titanium (0.25%/K) [7] and vanadium oxide (2–3%/K) [8], and highly boron-doped a-Si (2%/K) [9], the a-Si TFT shows higher temperature sensitivity. Apart from this, because the a-Si TFT has a lower thermal budget, it can be fabricated below 350 °C by using standard IC processes without destroying the pre-formed ICs, which is an important precondition of post-CMOS micromachining process.

Porous silicon micromachining was used to fabricate the NiCr–Au metallic bolometer with a thermally well-isolated air bridge by Lang et al. [10]. Compared with traditional surface micromachining such as polyimide and polysilicon-based, and bulk micromachining either of front-side or of back-side, this approach can not only obtain the thermal isolation structure with a deep air gap, but also breakthrough the geometrical limitations of the membrane and reduce the releasing time. However, there are few reports on the integration schemes of combining a standard IC process sequence for forming smart electronics with porous silicon micromachining process. Therefore, this paper also describes an improved porous silicon micromachining technology to fabricate the thermal isolation structure of the a-Si TFT-based IR sensor.

2. Thermal characteristics of a-Si TFTs

Thermal characteristics of a-Si TFTs have little been exploited for thermal sensors. We employ the a-Si TFT as the

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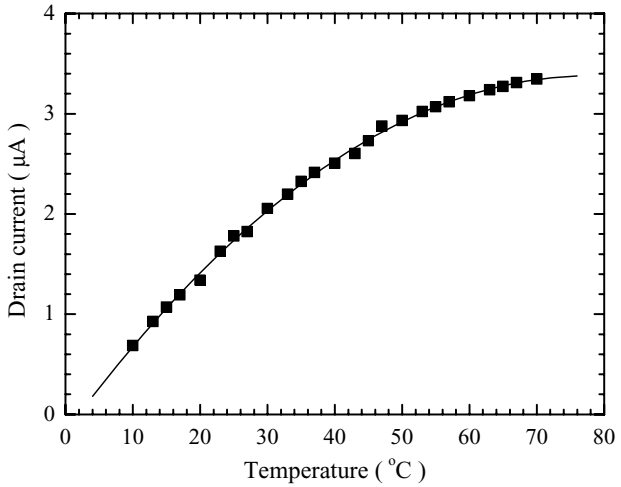

Fig. 1. Measured results of the drain current vs. temperature of a fabricated p-type a-Si TFT.

sensing element due to its high temperature coefficient of drain current (TCC):

$$\alpha_i = \frac{1}{I_{ds}} \times \frac{dI_{ds}}{dT} \quad (1)$$

where I_{ds} is the drain current of the TFT, and T the absolute temperature in K. The expression of TCC can be derived from a simple electrical model of the TFT working in saturation region [11], and is given by:

$$\alpha_i = \left(\frac{1}{T} + \frac{E_a}{kT^2}\right) - \left(\frac{-|V_t|}{|V_{gs} - V_t|}\right) \times \frac{E_c - E_F}{kT^2} \quad (2)$$

where k is the Boltzmann's constant, V_t the threshold voltage, V_{gs} the applied voltage across gate and source electrodes, and E_a, E_c and E_F the activation energy, the conduction band edge energy and the Fermi energy of the a-Si, respectively.

In Eq. (2), the first part is a positive value that represents the temperature dependence of carrier mobility of the a-Si in channel region, while the second part (not including the minus sign) is a negative value that represents the temperature dependence of threshold voltage of the a-Si TFT. It is indicated that the drain current increases with temperature, and both the carrier mobility shift and the threshold voltage shift contribute to the large value of TCC. It should be pointed out that as temperature increases, the carrier mobility of the a-Si in channel region increases because of the thermal activation of carriers at room temperature, which is essentially different from that of the crystalline silicon in MOSFETs.

When the temperature is increased by ΔT, the drain current is consequently changed by $\alpha_i I_{ds} \Delta T$. Fig. 1 shows the measured results of the drain current versus temperature of a fabricated p-type a-Si TFT at $V_{gs} = -7.5$ V and $V_{ds} = 1.5$ V. The ratio of channel width to length (W/L) is 100 μm/8 μm. The measured threshold voltage and the carrier mobility are about -2.8 V and 0.35 cm^2/V s, respectively. By using

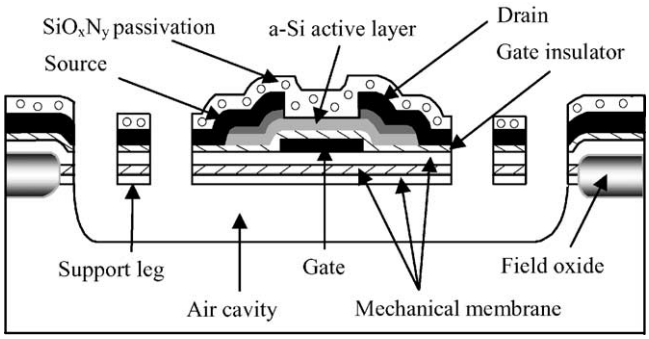

Fig. 2. Cross-sectional view of a-Si TFT-based uncooled IR sensors.

Eq. (1) and measuring the drain current at various temperature, a TCC value of about 4.8%/K is achieved at 23 °C, suggesting the a-Si TFT is an attractive candidate for the sensing element of uncooled IR sensors.

3. Sensor structures

The cross-sectional view of the a-Si TFT-based uncooled IR sensor is shown in Fig. 2. In this design, the a-Si TFT, i.e. the sensing element of the sensor, is placed at a thermally well-isolated air bridge suspending above the silicon substrate, which can limit the heat loss and maximize the temperature increase caused by the absorption of IR radiation. The height of the air cavity between microbridge and substrate is 7.5 μm. It is observed that the inverted-staggered TFT is used, which has the bottom gate electrode, and the source/drain electrodes and the gate electrode are on opposite sides of the active layer. This type of TFT is preferred, since the bottom gate electrode can serve as a reflecting mirror. Thus, the incident IR radiation will be reflected at the gate metal and be absorbed twice by absorptive materials. For certain spectral bands in region of 8–14 μm, no additional material for enhancing IR absorption is needed, since the SiO_xN_y passivation layer of the a-Si TFT has good IR absorptions due to Si–O bonds (8–10 μm) and Si–N bonds (11–13 μm) [12]. Numerical calculations show an absorptance of over 60% can be achieved in region of 8–14 μm.

4. Performance expressions

The performance of IR sensors is characterized by certain figures of merit such as responsivity R_V, detectivity D^* and noise-equivalent temperature difference NETD. A single circuit shown in Fig. 3 is used to obtain the performance expressions of our a-Si TFT-based IR sensors, which converts the variations of the drain current into voltage signals.

The responsivity R_V is defined as the output signal voltage divided by the input IR radiation power falling on the sensor

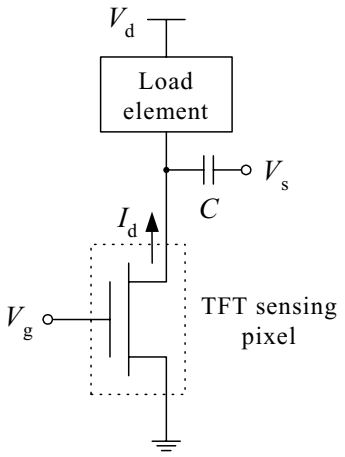

Fig. 3. Single circuit for analyzing performance equations of a-Si TFT-based uncooled IR sensors.

surface. The responsivity R_V can be expressed as:

$$R_V = \frac{\eta \alpha_i I_{ds} R_d}{G_{th}\sqrt{1 + 4\pi^2 f^2 \tau^2}} \quad (3)$$

where η is the IR absorptance of the sensor, R_d the a-Si channel resistance, G_{th} the total thermal conductance, f the frequency of the modulation signal, and τ the thermal time constant defined by the ratio of the sensor's thermal capacitance C_{th}, to the thermal conductance G_{th}, C_{th}/G_{th}. Therefore, for high responsivity, high η, high α_i, low G_{th} and low $f(2\pi f\tau << 1)$ are required.

The detectivity D^* is an area-normalized parameter which takes into account the noise of the sensor as well as its responsivity, and is given by:

$$D^* = \frac{R_V\sqrt{A_D \Delta f}}{V_n}, \quad (4)$$

where A_D is the area of the sensing pixel, Δf the measurement bandwidth, and V_n the noise voltage. In general, the noise voltage is determined by the sum of the contributions due to the background noise, the temperature fluctuation noise, and the noise produced by the sensing pixel, which is made up of the Johnson noise and low frequency ($1/f$) noise. We can observe that to achieve a high D^*, the device must have large value of R_V as well as low noise voltage.

The noise-equivalent temperature difference NETD is defined as the increase of temperature of the IR source over reference temperature T_{REF} that produces signal-to-noise ratio of 1 in IR sensors. It can be derived from the measured V_n and R_V through the following equation [13]:

$$\begin{aligned} V_n &= R_V[P(T_{REF} + \mathrm{NETD}) - P(T_{REF})] \\ &= R_V \frac{\varepsilon\sigma}{\pi l^2} A A_D[(T_{REF} + \mathrm{NETD})^4 - T_{REF}^4] \end{aligned} \quad (5)$$

where $P(T)$ is the incident power falling on the sensor surface at a blackbody temperature T, ϵ the emissivity, α the Stefan–Boltzmann constant ($5.67 \times 10^{-8}\,\mathrm{Wm^{-2}\,K^{-4}}$), A the aperture area of the blackbody, and l the distance from the aperture to the sensor.

5. Fabrication process

In order to implement an integrated a-Si TFT-based IR sensor, we have developed the monolithic process flow based on n-MOSFET IC process and porous silicon micromachining process.

Since silicon wafers with low resistivity ($\rho < 1$ ohm cm) are not suitable for MOSFETs formation, the (100)-oriented, 30-50 ohm cm, p-type wafers are used as starting substrates, although porous silicon can be easily achieved within the low resistivity wafers. The major fabrication steps are shown in Fig. 4, and are described as follows:

(1) First, a composite membrane consisting of 100 nm thick silicon oxide (SiO_2) and 150 nm thick silicon nitride (Si_3N_4) was deposited by LPCVD as the masking layer against hydrofluoric acid in porous silicon formation step. In order to easily prepare porous silicon within substrates, heavily doped p^+ regions were selectively formed by ion implanting ($5 \times 10^{l5}\,\mathrm{cm^{-2}}$ boron at 100 keV) and thermal drive-in (7 h at 1150 °C) procedures with the resultant deep junctions to a depth of 7.5 μm. After removal of Si_3N_4 and SiO_2 from the back of the wafer, a p^+ contact layer was formed at this surface by implanting boron at 70 keV with a dose of $5 \times 10^{15}\,\mathrm{cm^{-2}}$ and annealing at 950 °C for 30 min. The porous silicon formation was then carried out in a solution of 20 wt.% HF, 30% water and 50% alcohol with a constant current of $30\,\mathrm{mA\,cm^{-2}}$ for 8 min. The thickness of the prepared porous silicon layer was about 7.5 μm (Fig. 4(a)).
(2) After porous silicon formation, the wafers were immersed into 40 wt.% HF solution for 80 min to remove the masking layer. We should point out that, in the subsequent process such as field oxide growth, if the porous silicon was exposed to high temperature and left unsealed, it would be oxidized and even destroyed. Therefore, a protection layer consisting of 50 nm thick SiO_2 and 150 nm thick Si_3N_4 was deposited by LPCVD and patterned to seal the porous silicon surface (Fig. 4(b)).
(3) The n-MOS circuits were then fabricated with a standard single polysilicon, single metal n-MOS process. A 600 nm thick LPCVD-SiO_2 was deposited over the circuit to form a flat surface (Fig. 4(c)).
(4) Next, the fabrication of a-Si TFTs was carried out. In this step, a 400 nm thick aluminum (Al) was deposited over the wafer by sputtering, and then patterned for gate electrodes of a-Si TFTs. After a 300 nm thick SiN_x, a 150 nm thick undoped a-Si and a 30 nm thick boron doped a-Si were deposited by PECVD at 300 °C without breaking the vacuum of the reactive chamber, the two deposited a-Si films were patterned and dry-etched, followed by

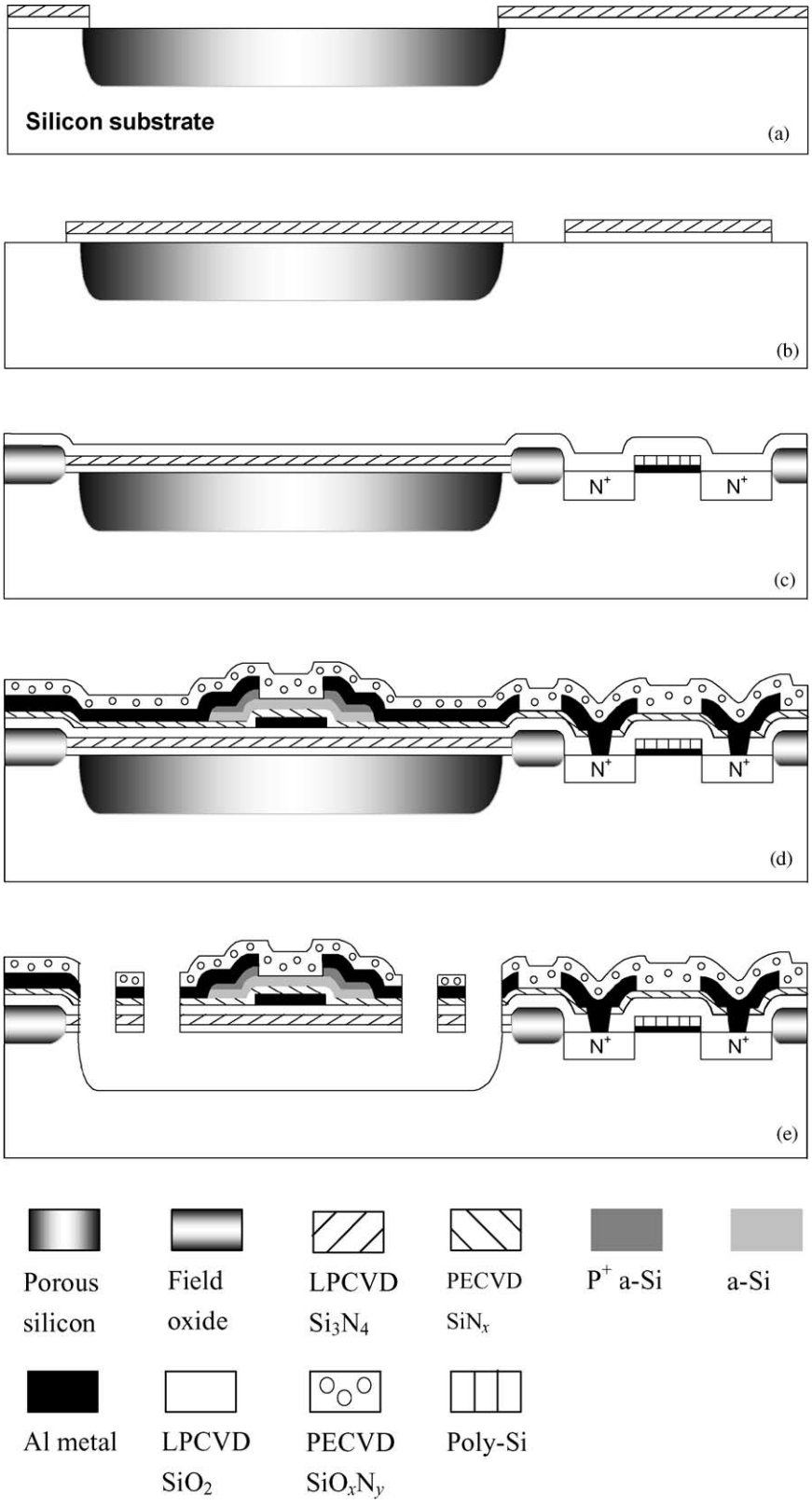

Fig. 4. Major process flow for a-Si TFT-based uncooled IR sensors.

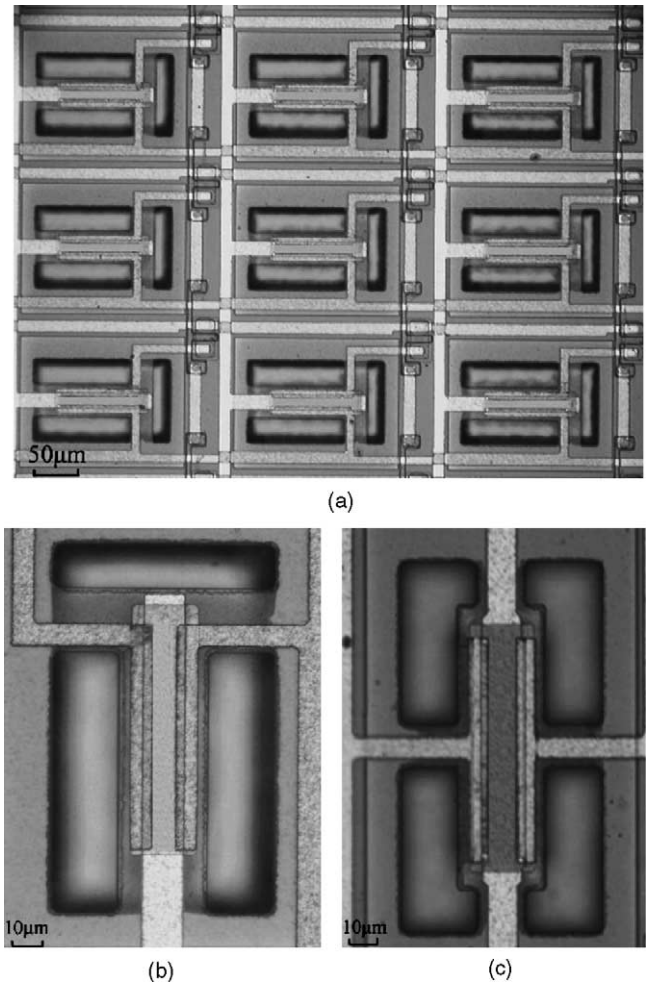

Fig. 5. Optical images of (a) sensor array and (b) single sensor.

opening the holes contacting to n-MOSFETs. A 1.0 μm thick Al was deposited by sputtering, and then patterned to form the source/drain electrodes of a-Si TFTs and the electrical connections of circuits. The doped a-Si between the drain and source electrode dry etched. After deposition of 800 nm thick SiO_xN_y passivation layer by using PECVD at 300 °C, an annealing procedure was performed at 350 °C for 40 min in the hydrogen atmosphere (Fig. 4(d)).

(5) Finally, etching holes were patterned and dry-etched until the top surface of the porous silicon appeared. The porous silicon sacrificial layer was released through the etching holes in a solution of 5 wt.% tetra-methyl-ammonium-hydroxide solution, 1.6 % dissolved silicon powder and 0.6% $(NH_4)2S_2O_8$ at 85 °C. The releasing time was 12 min (Fig. 4(e)).

We have fabricated the integrated a-Si TFT-based IR sensor with different geometrical configurations and various ratio of *W*/*L*. The freestanding air bridges were formed with a yield of almost 100%. Fig. 5 shows the optical images of (a) the part of sensor arrays and (b–c) single sensors.

6. Tests and results

The IR detection figures of merit were found optically at atmospheric pressure and room temperature (23 °C). The test sample is shown in Fig. 5(b) with a dimension of 150 μm × 90 μm and a *W*/*L* ratio of 100 μm/8 μm. The fabricated sensor was connected in series with a low noise battery (constant-voltage source, −10 V) and to a load resistor with $V_{gs} = -7.5$ V and $V_{ds} = -7.5$ V. Since the TFT had a threshold voltage of −2.8 V, it worked in the saturation region. The sensor was then exposed to the radiation of a calibrated blackbody heated at temperatures ranging from 400 to 900 °C. The incident radiation was filtered by a window with spectral region of 8–14 μm transmittance modulated by a mechanical chopper. The signal voltage V_s was measured using a lock-in amplifier with a bandwidth of 1 Hz. The noise voltage V_n of the sensor was measured using the same measuring system without blackbody illumination.

As a first step, we measured the thermal characteristics of the fabricated p-type a-Si TFT. The results have been described in Section 2. In short, the value of TCC is 4.8%/K at 23 °C, and the drain current is 1.63 μA with a dc channel resistance of 4.6 MΩ at $V_{gs} = -7.5$ V and $V_{ds} = -7.5$ V.

In order to determine the responsivity, the power response of the sensor was measured. Fig. 6 shows the signal voltage as a function of the IR radiation power at a frequency of 30 Hz. The radiation power *P* is adjustable by changing the temperature of the blackbody, and is calculated from the equation of $P = \epsilon\alpha A A_D T^4/(\pi l^2)$. It is indicated that the sensor has a linear voltage response with the incident power. The responsivity R_V of 40.5 kV/W at a frequency of 30 Hz is obtained from the slope of the linear fit line.

The thermal time constant of the sensor was evaluated by measuring the responsivity at different chopping frequencies and determining the cut-off frequency. Fig. 7 shows the dependency of the responsivity on frequency of the sensor. As expected from Eq. (3), the frequency response of R_V

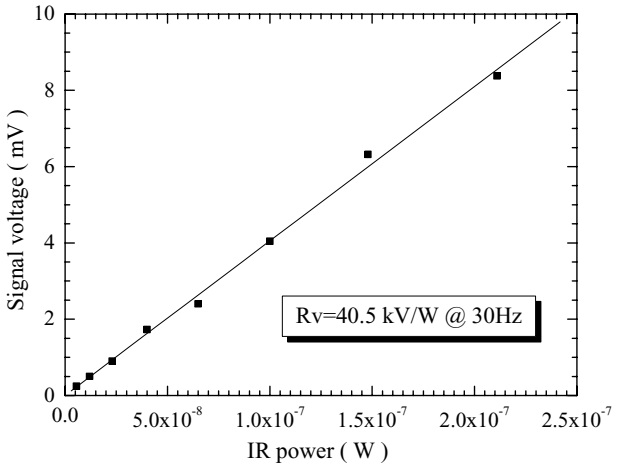

Fig. 6. Dependency of signal voltage on IR radiation power at a frequency of 30 Hz.

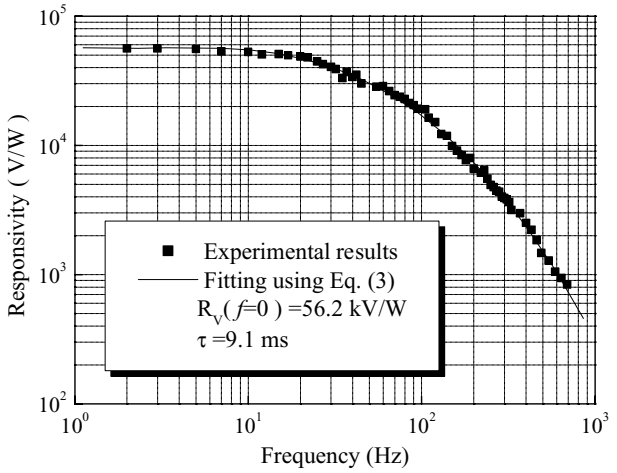

Fig. 7. Dependency of responsivity on chopping frequency.

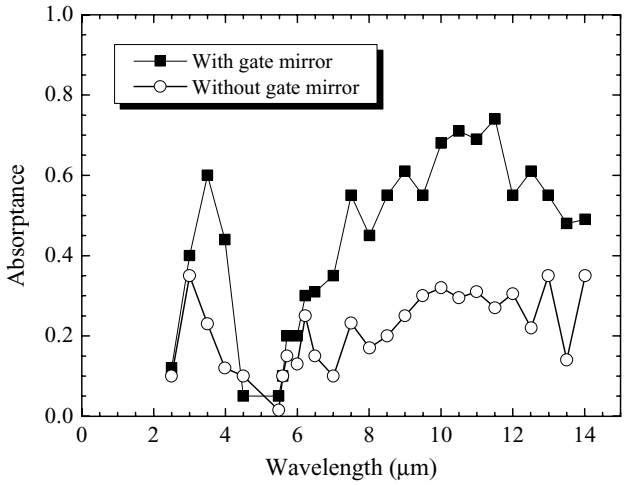

Fig. 9. Measured IR absorptance in spectrum region of 2.5–14.5 μm.

is almost flat at low frequencies, while decreases at high frequencies with a cut-off frequency of 110 Hz. Hence, a thermal time constant of about 9.1 ms is obtained, which is suitable for the frequency response required for 30 Hz imaging applications. Using Eq. (3), the best fits correspond to a high dc responsivity ($f = 0$) of 56.2 kV/W.

Since having a high responsivity alone was not that important, noise voltage were also investigated to evaluate the performance of the sensor in terms of detectivity. Fig. 8 shows the dependency of the noise voltage and the detectivity on frequency of the sensor. The noise voltage distinctly decreases with the frequency until 100 Hz is reached, which is a typical characteristic of a $1/f$ like noise. The $1/f$ noise sources in a-Si TFTs are associated with the intrinsic channel and the access resistances. At a frequency of 30 Hz, the noise voltage is around 1.83 μV with a resultant detectivity of 2.7×10^8 cm $Hz^{1/2}$ W^{-1} It is observed that the noise voltage is relatively low at frequencies of over 100 Hz, since the thermal noise dominates over the $1/f$ noise at high frequencies. The maximum detectivity of 3.4×10^8 cm $Hz^{1/2}$ W^{-1} is achieved at a frequency of 22 Hz. From the point of view of detectivity, the optimum range for chopping frequency would be 10–100 Hz above which the detectivity tends to fall to low values. According to Eq. (5), the value of NETD calculated for a reference temperature of 23 °C (296 K) is approximately 90 mK at a frequency of 30 Hz. This value is comparable to the results of a-Si resistive bolometers [14] and PVDF pyroelectric sensors [3].

Fig. 9 shows the measured IR absorptance of the sensor. For comparison, an identical multi-layer structure except without Al-gate electrode was fabricated to test the IR absorption. The absorptance of the sensor can reach 42–70% in spectrum region of 8–14 μm, while the test structure only has an absorptance of 18–37%. Hence, the Al-gate electrode can improve the IR absorptance of the sensor due to its reflecting effect.

When the sensor arrays are used in thermal imaging applications, the sensitivity distribution of the arrays should be

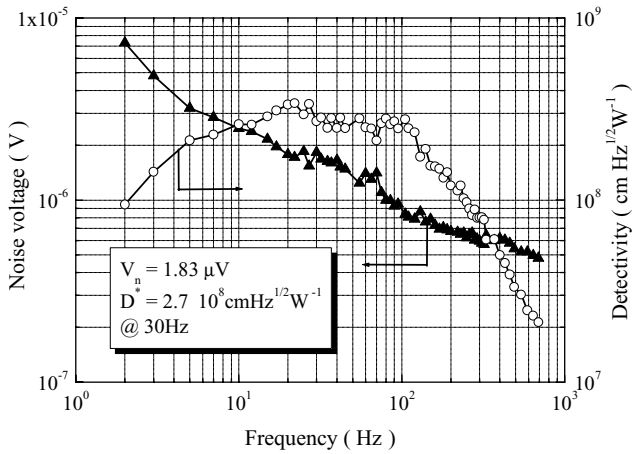

Fig. 8. Dependency of noise voltage and detectivity on chopping frequency.

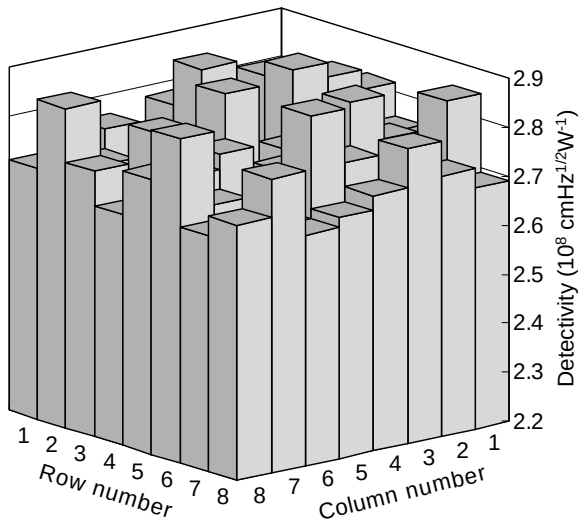

Fig. 10. Distribution of detectivity of an 8 × 8 a-Si TFT-based uncooled IR sensor array.

determined in order to obtain the compensation quantity of each pixel. Fig. 10 displays the distribution of the detectivity of an 8 × 8 a-Si TFT-based IR sensor array. The detectivity of each pixel is measured at a frequency of 30 Hz. It indicates that the intrinsic uniformity of the array is less than 5% with the average detectivity of 2.74 cm $Hz^{1/2}$ W^{-1}.

It should be pointed out that the results of the a-Si TFT-based IR sensor reported here are preliminary. The performances can be further improved by optimizing the dc bias voltage of the TFT and the geometric configuration of the air bridge.

7. Conclusions

We have successfully fabricated a-Si TFT-based uncooled IR sensors integrated with n-MOSFETs. The a-Si TFT is a prospective candidate for IR sensors due to its high temperature coefficient of drain current of 4.8%/K. The porous silicon micromachining technique has been developed to fabricate the thermal isolation structure, which is compatible with the standard IC process. The sensor has a responsivity of over 40 kV/W, a detectivity of over 10^8 cm $Hz^{1/2}$ W^{-1}, a thermal response time of 9.1 ms and a noise equivalent temperature difference of below 0.1 °C. The intrinsic uniformity of the 8 × 8 sensor array is less than 5%.

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