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Freestanding a-Si Thin Film Transistor for Room-Temperature Infrared Detection *

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We present the fabrication and characterization of a novel uncooled infrared sensor for room-temperature infrared imaging. The sensitive element of the sensor is a freestanding amorphous silicon thin film transistor (a-Si TFT) with the temperature coefficient of the drain current (TCC) of 0.015–0.08/K. The TCC value is sensitive to the ambient temperature and can be controlled by the gate voltage of the a-Si TFT. The complete procedures based on the porous silicon micromachining technique for fabricating thermally isolated air bridges are described. The isolation structures have a thermal conductance of 5×10^{-6} *W/K and a thermal capacitance of* 4.9×10^{-8} *J/K. The effects of the gate voltage on the performance figures such as responsivity, noise voltage and detectivity are described and analysed in detail. The maximum detectivity reaches* 4.33×10^{8} *cmHz*$^{1/2}$*W*$^{-1}$ *at a chopping frequency of 27 Hz and a gate voltage of* -15 *V.*

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Infrared (IR) imaging plays an important role in civilian and military applications such as night vision, biomedical diagnostics, thermal probing of active microchips and fire detection. Recently, advances in micro-electro-mechanical-system (MEMS) technologies have led to the development of highly sensitive thermal sensors that can be employed as uncooled IR sensors. The elimination of cryogenic cooling and the feature of relatively flat broadband spectral response can make the uncooled IR sensors very promising.

There are several families of available uncooled IR sensors, such as resistive or dielectric bolometers,[1-3] pyroelectrics,[4] thermopiles,[5] and other solid-state sensors.[6] In this Letter, we present a different approach to IR detection using amorphous silicon thin film transistors (a-Si TFTs) as sensitive elements. An important reason why the a-Si TFT is useful for IR detection is that amorphous silicon TFTs possess a sensitive temperature dependence of drain current.[7] The measured temperature coefficient of drain current (TCC) of the fabricated a-Si TFT is about 0.015–0.08/K at room temperature. Compared to the temperature coefficient of resistance (TCR) values of some typical materials such as titanium (0.0025/K),[8] vanadium oxide (VO_x) (0.02–0.03/K),[9] and highly boron-doped a-Si (0.02/K),[10], the a-Si TFT exhibits higher temperature sensitivity. On the other hand, the a-Si TFT can be fabricated below 350°C by using standard integrated circuit (IC) processes without destroying the preformed ICs, which is an important precondition for the post-IC micromachining process.

Figure 1 shows the structure of an a-Si TFT-based IR sensor. The operation of the sensor is based on conversion of incident IR radiation energy into temperature increase, which in turn changes the drain current of the a-Si TFT related into its TCC value. The attractive features of the sensor are: (i) a freestanding a-Si TFT is used as the sensitive element; (ii) in order to reduce the thermal contact between the TFT and its surroundings and to increase the sensitivity, silicon underneath the TFT is removed using porous silicon micromachining to form a thermally well-isolated air bridge; (iii) the bottom-gate structured a-Si TFT is preferred, since the gate metal can serve as a reflecting mirror, at which the IR radiation is reflected and can be absorbed twice by absorptive materials; (iv) no additional material for enhancing IR absorption is needed, since the SiON passivation layer has good IR absorptions in the region of 8–14 μm due to Si–O bonds (8–10 μm) and Si–N bonds (11–13 μm).[11]

The fabrication process starts with a 3-inch, 30–50 ohm-cm, p-type (100) silicon wafer. The fabrication steps are briefly described as follows. Initially, the 7.5 μm deep p^+ wells were selectively formed in the patterned silicon substrates by ion implanting and thermal drive-in procedures. Then, the porous silicon sacrificial layer was prepared in the p^+ wells by conventional anodic electrochemical reactions. After a composite layer of 100-nm SiO_2 and 150-nm Si_3N_4 was deposited to protect the porous silicon, the fabrication of the a-Si TFTs were carried out. In this step, the 400-nm-thick aluminium was deposited and patterned for the gate electrode. The transistor has an insulator of 300-nm-thick SiN, an active layer of 150-nm-thick undoped a-Si, an electrical contact layer of

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30-nm-thick boron doped a-Si and a passivation layer of 800-nm-thick low-stress SiON. Those silicon-based films for the transistor were deposited by plasma enhanced chemical vapour deposition (PECVD) at the same temperature of 300°C. Finally, the porous silicon sacrificial layer was removed in a tetra-methyl-ammonium-hydroxide (TMAH) solution (5%, 85°C) via etching holes to form the thermal isolation structures.

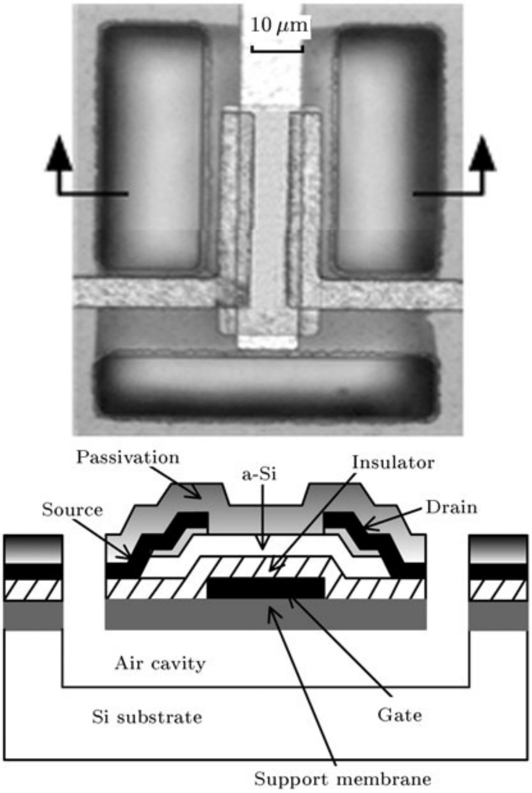

Fig. 1. Structure of an a-Si TFT-based IR sensor: (a) top view of optical image and (b) cross-sectional drawing.

As shown in Fig. 1(a), the size of the fabricated sensor is 150 μm×90 μm, and the channel length of the TFT is 8 μm with a width/length = 12.5/1. The height of the air cavity between the air bridge and the substrate is 7.5 μm which is determined by the depth of the p^+ well.

The thermo-electrical characterization of the fabricated p-type a-Si TFT was performed using HP4260 Semiconductor parameter with a closed cryostat at atmospheric pressure. The drain current I_{ds} with respect to temperature T was measured over a wide temperature range from 10 to 70°C. The TCC value was calculated with $dI_{ds}/(I_{ds}dT)$. Figure 2 presents the typical temperature dependence of I_{ds} and the TCC value when both the gate voltage V_g and the drain voltage V_{ds} of the a-Si TFT are -7.5 V. It is shown that the increase of temperature causes the a-Si TFT to exhibit higher drain current. At 296 K (23°C), the a-Si TFT has a drain current of 1.63 μA with a TCC value of 0.048/K. It is observed that the TCC value is sensitive to temperature change, decreasing from 0.06 to 0.015/K with the increase of the temperature.

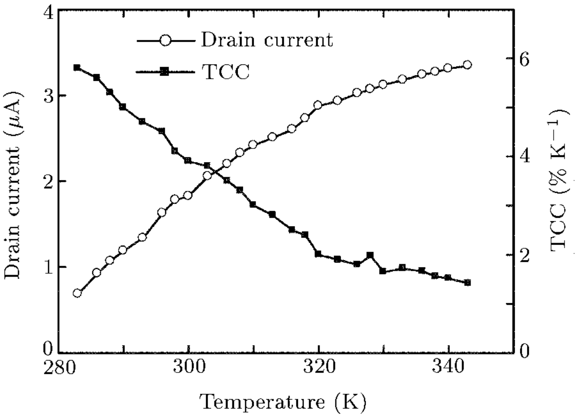

Fig. 2. Typical temperature dependence of the drain current and TCC value.

We have investigated the effects of the gate voltage on the TCC value. In this experiment, V_g was varied from -1 to -15 V, while V_{ds} was fixed at -7.5 V. The TCC value was calculated based on the $I_{ds} - T$ measurement for different V_g. The threshold voltage V_t of -2.8 V was derived from the I_{ds}–V_g measurement. Figure 3 displays the measured TCC value for 23°C with respect to V_g. The TCC value decreases with increasing $|V_g|$. The measured TCC value for $V_g = -1$ V is 8.3%/K dropping to a value of -2.8%/K for $V_g = -15$ V. This result can be attributed to the adjustable channel resistance R_d of the a-Si TFT that undergoes an off-state below threshold to an on-state above the threshold. The self-heating of the a-Si TFT at higher $|V_g|$ results in a reduction of R_d, with a consequent degradation of the TCC value. We believe that the a-Si TFT above the threshold with a moderate TCC value is preferred for the sensitive element in view of the limitation of noise, as will be described below.

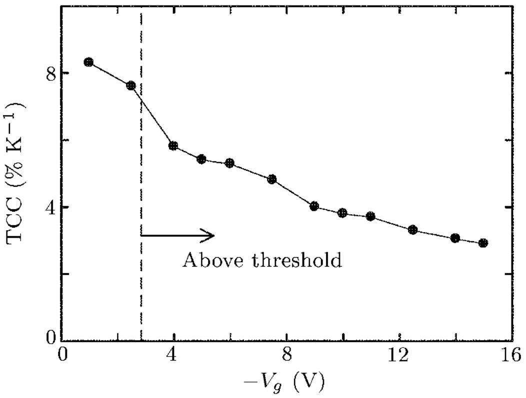

Fig. 3. TCC value versus gate voltage of the a-Si TFT.

Optical tests were performed to characterize the sensor using a set-up comprising a black body (700°C), a mechanical chopper and a lock-in amplifier. The sensor was connected to an adjustable load resistor with a low noise voltage source (-10 V). The load resistor converts the drain current variations into voltage signals. It should be pointed out that the dc static drain voltage of the a-Si TFT was biased at -7.5 V by adjusting the load resistance during the measurements.

The optical response of the sensor is expressed in terms of voltage responsivity R_V given by

$$R_V = \eta\beta I_{ds}R_L/\big[G_{\rm th}\sqrt{1+4\pi^2 f^2\tau_{\rm th}^2}\big], \qquad (1)$$

where η is the IR absorptivity, β is the TCC value, R_L is the load resistance, f is the chopping frequency, and $\tau_{\rm th}$ is the thermal time constant defined by the ratio of the sensor thermal capacitance $C_{\rm th}$ to its thermal conductance $G_{\rm th}$, $C_{\rm th}/G_{\rm th}$.

The responsivity was obtained by dividing the measured voltage response V_S by the incident IR power P. Figure 4 shows the measured responsivity with respect to the chopping frequency at different gate voltages. It is shown that R_V falls to low values at high frequencies ($f > 60$ Hz) due to the thermal time constant of the sensor. It is noted that R_V decreases with increase of $|V_g|$, which can be explained by using Eq. (1). Since the a-Si TFT has the dc static drain voltage of -7.5 V, the product of I_{ds} and R_L is a constant of -2.5 V. Therefore, R_V is directly proportional to the TCC value at a particular chopping frequency. At 30 Hz, the sensor has the responsivities of 70100, 47550, 40475, and 27489 V/W for the gate voltage of -2.5, -5, -7.5 and -15 V, respectively, which are almost in accordance with the corresponding TCC values at different V_g.

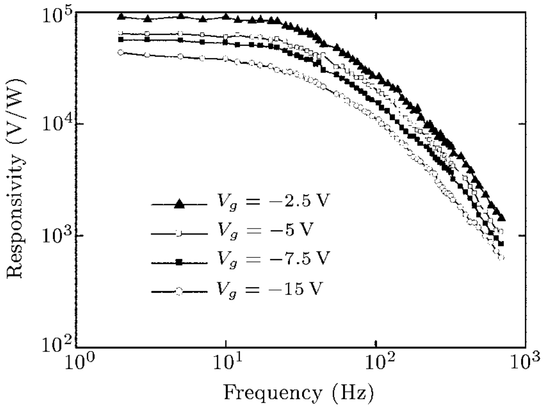

Fig. 4. Responsivity versus chopping frequency at different gate voltages.

The dc responsivity ($R_{V0} = \eta\beta I_{ds}R_L/G_{\rm th}$) and the thermal time constant of the sensor were obtained by fitting Eq. (1) to the measured responses. For example, R_{V0} and $\tau_{\rm th}$ for $V_g = -15$ V are extracted as 42.97 kV/W and 9.8 ms, respectively, which corresponds to $G_{\rm th}/\eta$ of 8.38×10^{-6} W/K. Since η is found to be 0.6 by measuring IR absorption spectra, $G_{\rm th}$ and $C_{\rm th}$ are extracted as 5×10^{-6} W/K and 4.9×10^{-8} J/K.

Figure 5 shows the noise voltage V_n of the sensor as a function of chopping frequency at different gate voltages. In all the cases of different gate voltages, V_n exhibits a $1/f$-like shape at low frequencies. The measured V_n for $V_g = -15$ V is 1.65 μV/Hz$^{1/2}$ at 10 Hz dropping to a value of 0.17 μV/Hz$^{1/2}$ at 700 Hz. Although the exact origin of noise needs to be further investigated, the $1/f$ noise originating from the sensor has a large contribution due to the noncrystalline structure of the amorphous silicon. The channel resistance of the a-Si TFT also serves as a good source of voltage fluctuations due to the Johnson noise given by $V_{nJ} = \sqrt{4kTR_d}$, where k is the Boltzmann constant. Since the measured R_d for $V_g = -15$ V is 1.066 MΩ, V_{nJ} is calculated to be about 0.133 μV/Hz$^{1/2}$ that is independent of frequencies and slightly below the total V_n of 0.17 μV/Hz$^{1/2}$, indicating that the Johnson noise dominates over the $1/f$ noise at high frequencies.

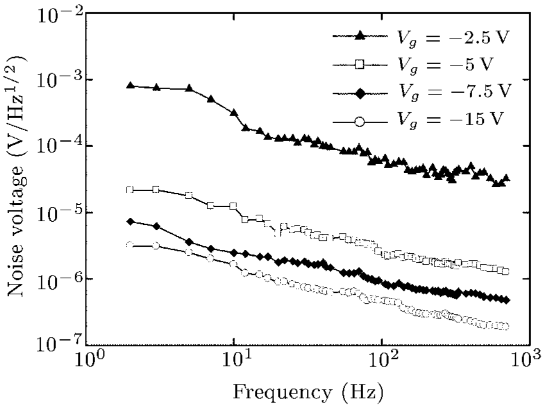

Fig. 5. Noise voltage versus chopping frequency at different gate voltages.

It is also observed in Fig. 5 that V_n decreases with increase of $|V_g|$. Because the a-Si TFT is below the threshold at $V_g = -2.5$ V, the high level of V_n for low gate voltage is mainly originated from the large channel resistance with excessive thermal noise. In the case of the above threshold, R_d decreases with V_g, resulting in the reduction of the thermal noise. The calculated value of V_{nJ} for $V_g = -2.5$ V is 18.37 μV/Hz$^{1/2}$, which is about 138 times higher than that for $V_g = -15$ V. On the other hand, the $1/f$ noise characteristics for different gate voltages can be explained by the Hooge relation:[12]

$$V_{1/f} \propto \frac{I_{ds}^b R_d}{\sqrt{Nf}}, \qquad (2)$$

where $V_{1/f}$ is the noise voltage, $b \approx 1$, and N is the number of charge carriers. Since the item $I_{ds}R_d$ maintains a constant of -7.5 V, $V_{1/f}$ is proportional to

$N^{-1/2}$. The higher $|V_g|$ can ensure more carriers in the channel of the a-Si TFT due to field effects, resulting in a degradation of the $1/f$ noise.

The detectivity ($D^* = R_V\sqrt{A\Delta f}/V_n$) gives the area-normalized signal-to-noise ratio in the detection frequency bandwidth Δf for the sensor with the area of A. Figure 6 shows the detectivity as a function of frequency at different gate voltages based on the above measurements of R_V and V_n. It is found that D^* increases with increasing V_g. For example, D^* for $V_g = -15$ V is approximately higher by two orders of magnitude than that for $V_g = -2.5$ V. The maximum D^* for $V_g = -15$ V reaches 4.33×10^8 cmHz$^{1/2}$W^{-1} at 27 Hz. Since imaging systems require sampling rate of 30 Hz or 60 Hz, it is meaningful that the sensor has approximately 98.8% of the maximum D^* at 30 Hz and 76% at 60 Hz. As is shown in Fig. 6, the optimum range for chopping frequency is about 20 to 120 Hz from the point of view of D^*. Compared to some IR sensors based on VO$_x$, a-Si and BaSrTiO$_3$ ferroelectric thin films, the performance of our sensor is comparable or better than them in terms of detectivity.

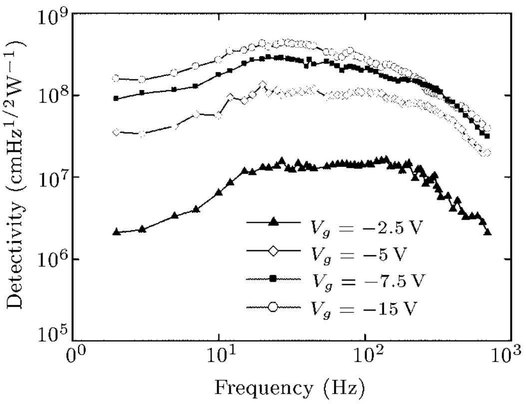

Fig. 6. Detectivity versus chopping frequency at different gate voltages.

It should also be pointed out that the sensors described in this Letter are not optimized. The thermal conductance of the suspending structure can be reduced further by employing a thinner membrane and a longer and narrower support leg with the resultant detectivity figure up to 10^9 cmHz$^{1/2}$W^{-1}.

In summary, a novel uncooled IR sensor based on a-Si TFT has been fabricated and characterized. The porous silicon micromachining has been combined with the high TCC properties of the a-Si TFT. The TCC value of the a-Si TFT is sensitive to temperature change, decreasing from 0.06 to 0.015/K with the increase of the temperature, and it is also controlled by the gate voltage due to adjustable channel resistance. As $|V_g|$ is increased, the responsivity and the noise voltage decrease, while the detectivity increases for a fixed drain voltage of -7.5 V. The sensor has a thermal time constant of less than 9 ms and a maximum detectivity of 4.33×10^8 cmHz$^{1/2}$W^{-1} at 27 Hz and $V_g = -15$ V. The experimental results indicate the freestanding a-Si TFT is a promising candidate for uncooled IR sensor and IR imaging applications.

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